I CLAIM:

1. A semiconductor package comprising:

a semiconductor die having a pad-mounting surface, and a plurality of spaced apart bonding pads formed on said pad-mounting surface;

a plurality of conductive bodies, each of which has a trace part that is formed on said pad-mounting surface and that is offset from a respective one of said bonding pads in a lateral direction relative to said pad-mounting surface, and a pad-connecting part that extends from said trace part to connect electrically with the respective one of said bonding pads;

a dielectric protective layer formed on said pad-mounting surface and said conductive bodies and formed with a plurality of bump-through-holes, each of which exposes a portion of said trace part of a respective one of said conductive bodies; and

a plurality of solder bumps, each of which fills a respective one of said bump-through-holes to connect electrically with said portion of said trace part of a respective one of said conductive bodies and each of which protrudes outwardly from said protective layer.

2. The semiconductor package of Claim 1, further comprising a plurality of metal plating layers, each of which is formed on a respective one of said bonding

pads, said pad-connecting part of each of said conductive bodies being formed on a respective one of said metal plating layers.

3. The semiconductor package of Claim 1, wherein each of said conductive bodies is made from conductive paste.

4. The semiconductor package of Claim 1, wherein said protective layer is made from epoxy resin.

5. The semiconductor package of Claim 1, wherein said trace part of each of said conductive bodies includes a metal layer that is electrically connected to a respective one of said solder bumps.

6. The semiconductor package of Claim 5, wherein said metal layer includes a nickel sub-layer and a gold sub-layer.

7. The semiconductor package of Claim 1, further comprising a pair of opposite dielectric partition walls that are formed on said pad-mounting surface at two opposite sides of each of said bonding pads, said trace part of each of said conductive bodies extending through a respective one of said partition walls in a transverse direction relative to said partition walls in such a manner that said pad-connecting part of each of said conductive bodies is disposed between said partition walls.

8. The semiconductor package of Claim 7, wherein said partition walls define an inner space therebetween,

said semiconductor package further comprising an encapsulant that fills said inner space so as to cover said bonding pads.

9. The semiconductor package of Claim 8, wherein said encapsulant is made from epoxy resin.

10. The semiconductor package of Claim 8, wherein said encapsulant is made from photo-sensitive ink.

11. The semiconductor package of Claim 8, wherein said encapsulant is made from polyimide.

12. The semiconductor package of Claim 8, wherein said partition walls have a height, which is measured from said pad-mounting surface, higher than that of said trace parts of said conductive bodies, said pad-connecting parts of said conductive bodies being covered by said encapsulant.

13. The semiconductor package of Claim 8, wherein said partition walls have a height, which is measured from said pad-mounting surface, substantially equal to that of said trace parts of said conductive bodies, said pad-connecting parts of said conductive bodies being exposed from said encapsulant.

14. The semiconductor package of Claim 1, further comprising a plurality of metal plating layers, each of which is formed on a respective one of said bonding pads, and a plurality of connection-enhancing bosses, each of which is formed on and protrudes from a respective one of said bonding pads, said pad-

connecting part of each of said conductive bodies being formed on a respective one of said metal plating layers and enclosing a respective one of said connection-enhancing bosses.

15. The semiconductor package of Claim 14, wherein each of said connection-enhancing bosses is made from a photoresist material.

16. A semiconductor package comprising:

a semiconductor die having a pad-mounting surface, and a plurality of spaced apart bonding pads formed on said pad-mounting surface;

a plurality of leads, each of which is attached to said pad-mounting surface at one side of a respective one of said bonding pads and each of which is spaced apart from the respective one of said bonding pads;

a plurality of conductive bodies, each of which electrically interconnects a respective one of said bonding pads and a respective one of said leads;

a dielectric protective layer formed on said pad-mounting surface and said leads and formed with a plurality of bump-through-holes, each of which exposes a portion of a respective one of said leads; and

a plurality of solder bumps, each of which fills a respective one of said bump-through-holes to connect electrically with said portion of a

respective one of said leads and each of which protrudes outwardly from said protective layer.

17. The semiconductor package of Claim 16, wherein each of said conductive bodies is a bonding wire.

18. The semiconductor package of Claim 16, wherein each of said conductive bodies is made from conductive paste.

19. The semiconductor package of Claim 16, wherein said protective layer is further formed with a plurality of pad-through-holes, each of which exposes a respective one of said bonding pads therefrom, said semiconductor package further comprising a plurality of encapsulants, each of which fills a respective one of said pad-through-holes so as to cover a respective one of said conductive bodies and a respective one of said bonding pads.

20. A semiconductor package comprising:

a semiconductor die having a pad-mounting surface, and a plurality of spaced apart bonding pads formed on said pad-mounting surface;

a printed circuit film including a film substrate that has a trace-forming surface, and a plurality of conductive traces that are formed on said trace-forming surface, said film substrate being formed with a plurality of bump-through-holes, each of which exposes a portion of a respective one of said conductive traces, said printed circuit film being

attached to said semiconductor die in such a manner that each of said conductive traces is electrically connected to a respective one of said bonding pads; and

a plurality of solder bumps, each of which fills a respective one of said bump-through-holes to connect electrically with said portion of a respective one of said conductive traces and each of which protrudes outwardly from said printed circuit film.

21. The semiconductor package of Claim 20, further comprising a plurality of metal plating layers, each of which is formed on a respective one of said bonding pads and extends therefrom to a periphery of the respective one of said bonding pads on said pad-mounting surface, each of said conductive traces being attached to a respective one of said metal plating layers at said periphery of the respective one of said bonding pads.

22. The semiconductor package of Claim 20, wherein said printed circuit film further includes an adhesive that is applied to said trace-forming surface for adhering with said pad-mounting surface of said semiconductor die.

23. A semiconductor package comprising:

a semiconductor die having a pad-mounting surface, and a plurality of spaced apart bonding pads

formed on said pad-mounting surface;

a printed circuit film including a film substrate that has a trace-forming surface and a back surface opposite to said trace-forming surface, said printed circuit film further including a plurality of conductive traces that are formed on said trace-forming surface, said film substrate being formed with a plurality of pad-through-holes, each of which is defined by a hole-defining wall, each of said conductive traces having an end portion that is disposed at a periphery of a respective one of said pad-through-holes on said trace-forming surface, said printed circuit film being attached to said semiconductor die in such a manner that said back surface of said printed circuit film is bonded to said pad-mounting surface of said semiconductor die and that each of said pad-through-holes exposes a respective one of said bonding pads therefrom;

a plurality of conductive layers, each of which is formed on said hole-defining wall of a respective one of said pad-through-holes and each of which is electrically connected to a respective one of said bonding pads and said end portion of a respective one of said conductive traces; and

a plurality of solder bumps, each of which is formed on a respective one of said conductive traces.

24. A method for making a semiconductor package, said

method comprising the steps of:

preparing a semiconductor die that has a pad-mounting surface, and a plurality of spaced apart bonding pads formed on said pad-mounting surface;

forming a plurality of conductive bodies, each of which has a trace part that is formed on said pad-mounting surface and that is offset from a respective one of said bonding pads in a lateral direction relative to said pad-mounting surface, and a pad-connecting part that extends from said trace part to connect electrically with the respective one of said bonding pads;

forming a dielectric layer on said pad-mounting surface and said conductive bodies;

patterning and etching said dielectric layer so as to form said dielectric layer into a pair of opposite dielectric partition walls that are disposed at two opposite sides of each of said bonding pads, said trace part of each of said conductive bodies extending through a respective one of said partition walls in a transverse direction relative to said partition walls in such a manner that said pad-connecting part of each of said conductive bodies is disposed between said partition walls, said partition walls defining an inner space therebetween;

filling said inner space with an encapsulant so as to cover said bonding pads;

forming a dielectric protective layer on said pad-mounting surface, said conductive bodies, and said encapsulant;

forming a plurality of bump-through-holes in said protective layer, each of said bump-through-holes exposing a portion of said trace part of a respective one of said conductive bodies; and

forming a plurality of solder bumps, each of which fills a respective one of said bump-through-holes to connect electrically with said portion of said trace part of a respective one of said conductive bodies, and each of which protrudes outwardly from said protective layer.

25. The method of Claim 24, further comprising forming a plurality of metal plating layers prior to formation of said conductive bodies, each of said metal plating layers being formed on a respective one of said bonding pads, said pad-connecting part of each of said conductive bodies being formed on a respective one of said metal plating layers.

26. The method of Claim 24, wherein said conductive bodies are made from conductive paste.

27. The method of Claim 24, wherein said encapsulant is made from epoxy resin.

28. The method of Claim 24, wherein said encapsulant is made from polyimide.

29. The method of Claim 24, wherein said encapsulant

is made from photo-sensitive ink.

30. The method of Claim 24, wherein said trace part of each of said conductive bodies includes a metal layer.

31. The method of Claim 30, wherein said metal layer includes a nickel sub-layer and a gold sub-layer.

32. The method of Claim 30, further comprising grinding said partition walls and said encapsulant prior to the formation of said dielectric protective layer in such a manner that said partition walls and said encapsulant have a height substantially equal to that of said trace part of each of said conductive bodies.

33. The method of Claim 25, further comprising forming a plurality of dielectric connection-enhancing bosses prior to formation of said conductive bodies, each of said connection-enhancing bosses being formed on a respective one of said metal plating layers, said pad-connecting part of each of said conductive bodies being formed on the respective one of said bonding pads and a respective one of said connection-enhancing bosses in such a manner that said pad-connecting part encloses the respective one of said connection-enhancing bosses so as to prevent said pad-connecting part from peeling from the respective one of said bonding pads.

34. A method for making a semiconductor package, said

method comprising the steps of:

preparing a semiconductor die that has a pad-mounting surface, and a plurality of spaced apart bonding pads formed on said pad-mounting surface;

forming a plurality of conductive bodies, each of which has a trace part that is formed on said pad-mounting surface and that is offset from a respective one of said bonding pads in a lateral direction relative to said pad-mounting surface, and a pad-connecting part that extends from said trace part to connect electrically with the respective one of said bonding pads;

forming a dielectric layer on said pad-mounting surface and said conductive bodies;

grinding said dielectric layer to an extent where said conductive bodies are exposed therefrom;

forming a dielectric protective layer on said pad-mounting surface and said conductive bodies;

forming a plurality of bump-through-holes in said protective layer, each of said bump-through-holes exposing a portion of said trace part of a respective one of said conductive bodies; and

forming a plurality of solder bumps, each of which fills a respective one of said bump-through-holes to connect electrically with said portion of said trace part of a respective one of said conductive bodies, and each of which protrudes

outwardly from said protective layer.

35. The method of Claim 34, wherein said trace part of each of said conductive bodies includes a metal layer.

36. The method of Claim 35, wherein said metal layer includes a nickel sub-layer and a gold sub-layer.

37. The method of Claim 34, further comprising forming a plurality of pad-through-holes in said protective layer, each of said pad-through-holes exposing said pad-connecting part and an end portion of said trace part of a respective one of said conductive bodies, said method further comprising filling each of said pad-through-holes with an encapsulant to cover said pad-connecting part and said end portion of said trace part.

38. A method for making a semiconductor package, said method comprising the steps of:

preparing a semiconductor die that has a pad-mounting surface, and a plurality of spaced apart bonding pads formed on said pad-mounting surface;

forming a dielectric layer on said pad-mounting surface and said bonding pads;

patterning and etching said dielectric layer so as to form a plurality of trace-through-holes in said dielectric layer, each of said trace-through-holes having an end section that exposes a respective one of said bonding pads therefrom, and a trace section

that extends from said end section in a lateral direction relative to said pad-mounting surface;

forming a plurality of conductive bodies, each of which has a trace part that fills said trace section of a respective one of said trace-through-holes, and a pad-connecting part that extends from said trace part and that fills said end section of the respective one of said trace-through-holes to connect electrically with a respective one of said bonding pads;

forming a dielectric protective layer on said dielectric layer and said conductive bodies;

forming a plurality of bump-through-holes in said protective layer, each of said bump-through-holes exposing a portion of said trace part of a respective one of said conductive bodies therefrom; and

forming a plurality of solder bumps, each of which fills a respective one of said bump-through-holes to connect electrically with said portion of said trace part of a respective one of said conductive bodies, and each of which protrudes outwardly from said protective layer.

39. The method of Claim 38, further comprising forming a plurality of pad-through-holes in said protective layer, each of said pad-through-holes exposing said pad-connecting part and an end portion of said trace

part of a respective one of said conductive bodies, said method further comprising filling each of said pad-through-holes with an encapsulant to cover said pad-connecting part and said end portion of said trace part.

40. The method of Claim 38, wherein said trace part of each of said conductive bodies includes a metal layer.

41. The method of Claim 40, wherein said metal layer includes a nickel sub-layer and a gold sub-layer.

42. A method for making a semiconductor package, said method comprising the steps of:

preparing a semiconductor die that has a pad-mounting surface, and a plurality of spaced apart bonding pads formed on said pad-mounting surface;

forming a dielectric layer on said pad-mounting surface and said bonding pads;

patterning and etching said dielectric layer so as to form said dielectric layer into a plurality of strips, each of which has a pad-connecting segment that is connected to a respective one of said bonding pads, and an extension that extends from said pad-connecting segment and that is offset from the respective one of said bonding pads in a lateral direction relative to said pad-mounting surface;

forming a plating layer on each of said strips in such a manner that said plating layer has a

pad-connecting part which is formed on said pad-connecting segment of a respective one of said strips and which is electrically connected to a respective one of said bonding pads, and a trace part that extends from said pad-connecting part and that is formed on said extension of the respective one of said strips;

forming a dielectric protective layer on said pad-mounting surface and said plating layers on said strips;

forming a plurality of bump-through-holes in said protective layer, each of said bump-through-holes exposing a portion of said trace part of a respective one of said plating layers therefrom; and

forming a plurality of solder bumps, each of which fills a respective one of said bump-through-holes to connect electrically with said portion of said trace part of a respective one of said plating layers, and each of which protrudes outwardly from said protective layer.

43. The method of Claim 42, wherein said trace part of each of said plating layers includes a metal layer.

44. The method of Claim 43, wherein said metal layer includes a nickel sub-layer and a gold sub-layer.

45. A method for making a semiconductor package, said method comprising the steps of:

preparing a semiconductor die that has a pad-mounting surface, and a plurality of spaced apart

bonding pads formed on said pad-mounting surface;

attaching a plurality of leads on said pad-mounting surface, each of said leads being offset from a respective one of said bonding pads in a lateral direction relative to said pad-mounting surface, and having an end portion disposed adjacent to a respective one of said bonding pads;

forming a dielectric protective layer on said pad-mounting surface and said leads;

forming a plurality of bump-through-holes and a plurality of pad-through-holes in said protective layer, each of said bump-through-holes exposing a portion of a respective one of said leads therefrom, each of said pad-through-holes exposing said end portion of a respective one of said leads and a respective one of said bonding pads therefrom;

forming a plurality of conductive bodies, each of which is disposed in a respective one of the pad-through-holes and each of which electrically interconnects a respective one of said leads and a respective one of said bonding pads;

filling each of said pad-through-holes with an encapsulant to cover said conductive bodies and said bonding pads; and

forming a plurality of solder bumps, each of which fills a respective one of said bump-through-holes to connect electrically with said

portion of a respective one of said leads, and each of which protrudes outwardly from said protective layer.

46. The method of Claim 45, wherein each of said conductive bodies is a bonding wire.

47. The method of Claim 45, wherein each of said conductive bodies is made from a conductive paste.

48. A method for making a semiconductor package, said method comprising the steps of:

preparing a semiconductor die that has a pad-mounting surface, and a plurality of spaced apart bonding pads formed on said pad-mounting surface;

preparing a printed circuit film including a film substrate that has a trace-forming surface, and a plurality of conductive traces that are formed on said trace-forming surface, each of said traces having an end portion and an extension that extends from said end portion, said film substrate being formed with a plurality of bump-through-holes, each of which exposes a portion of said extension of a respective one of said conductive traces;

attaching said printed circuit film to said semiconductor die in such a manner that said trace-forming surface confronts said pad-mounting surface and that said end portion of each of said conductive traces is electrically connected to a respective one of said bonding pads and that said

extension of each of said traces is bonded to said pad-mounting surface and is offset from the respective one of said bonding pads in a lateral direction relative to said pad-mounting surface; and

forming a plurality of solder bumps, each of which fills a respective one of said bump-through-holes to connect electrically with said portion of said extension of a respective one of said traces, and each of which protrudes outwardly from said film substrate.

49. A method for making a semiconductor package, said method comprising the steps of:

preparing a semiconductor die that has a pad-mounting surface, and a plurality of spaced apart bonding pads formed on said pad-mounting surface;

preparing a printed circuit film including a film substrate that has a trace-forming surface and a back surface opposite to said trace-forming surface, and a plurality of conductive traces that are formed on said trace-forming surface, each of said traces having an end portion and an extension that extends from said end portion, said film substrate being formed with a plurality of pad-through-holes, each of which is disposed adjacent to said end portion of a respective one of said conductive traces and each of which is defined by a hole-defining wall;

attaching said printed circuit film to said

semiconductor die in such a manner that said back surface is bonded to said pad-mounting surface and that each of said pad-through-holes exposes a respective one of said bonding pads;

forming a plurality of conductive layers, each of which is formed on said hole-defining wall of a respective one of said pad-through-holes and each of which is electrically connected to a respective one of said bonding pads and said end portion of a respective one of said traces; and

forming a plurality of solder bumps, each of which is formed on said extension of a respective one of said traces.